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DATE: Monday, April 19, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L29	l24 and L27.ab.	11
☐	L28	l24 and L27	58
☐	L27	((automatic$9 or dynamic$9) near2 (chang$4 or alter$4 or modif$9 or switch$4) near3 (configur$9 or reconfigur$4))	1534
☐	L26	l6 and L24	4
☐	L25	l2 and L24	9
☐	L24	l15 or l16 or l17 or l18 or l19 or l20 or l21 or l22 or L23	6013
☐	L23	327/336.ccls.	487
☐	L22	327/334.ccls.	332
☐	L21	375/222.ccls.	2011
☐	L20	455/560.ccls.	448
☐	L19	365/185.03.ccls.	612
☐	L18	708/801.ccls.	321
☐	L17	713/100.ccls.	645
☐	L16	713/2.ccls.	798
☐	L15	713/1.ccls.	956
☐	L14	(configur$9 near2 register) same (analog adj function)	3
		DB=USPT; PLUR=YES; OP=OR	
☐	L13	5574678.pn.	1
☐	L12	5574678.pn.	1
☐	L11	5905398.pn.	1
☐	L10	5905398.pn.	1
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L9	L8 and (config$9 or reconfig$9)	3
☐	L8	((select$9 or choos$4 or choice) near3 (coupl$4 or decoupl$4) near3 (analog adj block))	3
☐	L7	L6 same (configur$4 or reconfigur$4)	20
☐	L6	l1 same analog	419
☐	L5	l1 same (analog adj function)	1
☐	L4	l1 same (analog adj block)	0
☐	L3	L1.ti.	6574

☐	L2	L1.ab.	8770
☐	L1	(multi-function$4 or ((plurality or multiple) near2 function) near2 device)	24359

END OF SEARCH HISTORY

L26: Entry 2 of 4 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6141376 A
TITLE: Single chip communication device that implements multiple simultaneous communication channels

Brief Summary Text (9):
Briefly the above and further objects of the present invention are realized by providing a single chip V.34 communications device responsive to control program commands that implement at least four V.34 communication channels simultaneously. The single chip V.34 communication controller implements both analog and digital standards simultaneously by using a pair of superscalar processors coupled to a multi-functional communication interface unit and a supportive memory system via a common communication bus.

Current US Original Classification (1):
375/222

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L14: Entry 2 of 3 File: EPAB May 2, 2002

DOCUMENT-IDENTIFIER: EP 1202184 A2
TITLE: Programming methodology and architecture for an analog programmable system on a chip

Abstract Text (1):
A method of programming a programmable analog device architecture that introduces on a single chip a set of tailored analog blocks and elements that can be configured and reconfigured in different ways to implement a variety of different analog functions. The analog blocks can be electrically coupled to each other in different combinations to perform different analog functions. The architecture includes an array of analog blocks, including continuous time blocks and different types of switched capacitor blocks. Each analog block includes analog elements that have changeable characteristics that can be specified according to the function to be performed. Configuration registers define the type of function to be performed, the way in which the analog blocks are to be coupled, the inputs and outputs of the analog blocks, and the characteristics of the analog elements. The configuration registers can be dynamically programmed. Thus, the device can be used to realize a large number of different analog functions and applications.

L7: Entry 6 of 20 File: USPT Aug 20, 2002

DOCUMENT-IDENTIFIER: US 6437830 B1
TITLE: System and data format for communicating data between a video decoder and a peripheral device

Detailed Description Text (12):
In an exemplary recording mode, decoder 110 provides high definition MPEG compatible digital video data representing a program to VCR 105 for recording. Decoder 110 configures VCR 105 to record the high definition MPEG data it receives in high definition format using configuration data conveyed in ancillary data in the VBI of the NTSC compatible composite video output by decoder 110 to VCR 105. VCR 105 is a multi-function unit capable of converting between different video formats both for recording and upon playback. For this purpose, VCR 105 contains an upsampling interpolator for converting SD video data to HD video data and a downsampling interpolator for converting HD video data to SD video data. VCR 105 also contains MPEG decoding/encoding and analog to digital and digital to analog conversion and sampling functions to convert between digital HD and SD data and analog composite video data. VCR 105 selects a signal recording format and converts the input signal data (HD, SD or composite analog) to the desired format for recording, in response to configuration and copy protection information received from decoder 110. VCR 105 also blocks recording or playback of prohibited material in response to the copy protection information.

L7: Entry 19 of 20 File: USPT Dec 1, 1981

DOCUMENT-IDENTIFIER: US 4303881 A
** See image for Certificate of Correction **
TITLE: Multi-function A.C. power meter

Detailed Description Text (17):
With the multi-gang rotary switch 7A, 8A, 10A, 34A, 35A, 36A, placed in the 7C, 8C, 10C, 34C, 35C, 36C positions respectively, the multi-function A.C. power meter is configured as a phase angle meter. In this configuration the compensated low pass active filters 5, 6, are bypassed, and the analog summing amplifier is connected as an summing amplifier. Refer to FIG. 1. ##EQU1## T26 is defined as the period of time the leading edge of the voltage waveform 17 at the output of the voltage squaring circuit 3, to the end of one complete cycle. Equation 7 and Equation 8 by integration reduce to e.sub.v =0.5T (Equation 9) and e.sub.i =(0.5T-t.sub.1)T (Equation 10).

Detailed Description Text (19):
With the multi-gang rotary switch 7A, 8A, 10A, 34A, 35A, 36A, placed in the 7D, 8D, 10D, 34D, 35D, 36D positions respectively, the multi-function A.C. power meter is configured as an A.C. watt meter and will measure true power. In this mode of operation, the analog summing amplifier 9 is configured as an phase detector and calibrated output amplifier mode, the same as for power factor measurements. The analog summing amplifier 9 is disconnected from the calibrated output indicator 12 and connected 13 to the scaled multiplier 14. The scaled multiplier 14 is an analog multiplier, which multiplies its inputs and gives a D.C. level output proportional to the product of the inputs. Refer to FIG. 3. The inputs to the scaled multiplier 14 come from the voltage input 1 and the current input 2. These inputs 1, 2, are individually scaled by scaling circuits 28 30, depending on their respective amplitudes and then rectified and filtered 29, 31. The resulting signals applied to the multiplier section 32 of the scaled multiplier 14 are K.sub.1 E.sub.v and K.sub.2 E.sub.i where K.sub.1 and K.sub.2 are the respective scaling factors. The output of the multipler section 32 will be E.sub.out =K.sub.1 K.sub.2 E.sub.v E.sub.i (Equation12). This signal is applied to the gain controlled output amplifier 33 of the scaled multiplier. The gain of this amplifier is linearly proportional to an applied voltage at its gain control input 13. The output of the analog summing amplifier is applied to this point. The final output of the scaling multiplier will then be E.sub.out =K.sub.1 K.sub.2 E.sub.v E.sub.i cos(p) (Equation 13).

Detailed Description Text (21):
With the multi-gang rotary switch 7A, 8A, 10A, 34A, 35A, 36A, placed in the 7E, 8E, 10E, 34E, 35E, 36E positions respectively, the multi-function A.C. power meter is configured as an apparent power meter. In this configuration both the inputs 7A, 8A, and the outputs 10A of the analog summing amplifier 9 are disconnected completely from the rest of the circuit. The scaled multiplier 14, functions identically as it does for measuring true power except that the gain control line 13 is set at unity gain. The output of the scaled multiplier will then be E.sub.out =K.sub.1 K.sub.2 E.sub.v E.sub.i (Equation 14). This equation is by definition the expression for apparent power, voltage times current (VA). The output 39 of the scaled multiplier 14 is applied to the calibrated output indicator.

L14: Entry 1 of 3 File: USPT Feb 6, 2001

DOCUMENT-IDENTIFIER: US 6185127 B1
TITLE: Selectable analog functions on a configurable device and method employing nonvolatile memory

Detailed Description Text (2):
FIG. 1 is an architectural diagram of a configurable microprocessor supervisory device 10 which employs a nonvolatile (NV) memory 11. Configurable microprocessor supervisory device 10 includes NV memory 11 having configuration registers 12-15, an x-to-y decoder 16, a first configuration 17, a second configuration 18, a third configuration 19, and an n configuration 20. Configurable microprocessor supervisory device 10 provides a range of analog functions and output levels which are selectable by programming the bits in NV register 12, 13, 14, and 15. Decoder 16 decodes through a line 21 of programmable bits in configuration register 12, a line 22 of programmable bits in configuration register 13, a line 23 of programmable bits in configuration register 14, or a line 24 of programmable bits in configuration register 15. The result of decoding configuration registers 12-15 produces a device configuration as either first configuration 17 via a line 25, second configuration 18 via a line 26, third configuration 19 via a line 27, and n configuration 20 via a line 28.

Detailed Description Text (4):
FIG. 2 is a flow chart of configurable microprocessor supervisory method 20 with non-volatile memory 11. A manufacturer or user selects 31 a certain combinations of analog functions and output levels for operation with a microprocessor (not shown). The combination of analog functions and output levels corresponds with first configuration 17, second configuration 18, third configuration 19, or n configuration 20. A manufacturer or user programs 32 certain nonvolatile bits in configuration registers 12, 13, 14, and 15 which correspond and enable the selected combinations of analog functions and output levels. An analog function or output level may have a range of settings. Optionally, when an analog function is enabled in step 32, the manufacturer or user programs 33 nonvolatile bits in configuration registers 12, 13, 14, and 15 to set a specific analog value associated with that enabled analog function. As a result of selecting the desirable combination of analog functions by programming configuration registers 12-15, first configuration 17, second configuration 18, third configuration 19, or n configuration 20 is generated on configurable microprocessor supervisory device 10.

Detailed Description Text (12):
Various control settings and modifications of configuration registers 12-15 are within the spirit of the present invention. For example, configuration registers 12-15 can be set at the factory and then locked so that a user just receives a standard part and is not aware that the part is programmable. Or, two configuration registers 12 and 13 can be accessed by a user with the other two configuration registers 14 and 15 are locked. Or, all four configuration registers 12-15 can be accessed by the user and then locked if the user choose to trim analog functions and to select a device interface among multiple possible interfaces.

Detailed Description Text (14):
The above embodiments are only illustrative of the principles of this invention and are not intended to limit the invention to the particular embodiments described.

For example, it is apparent to one skilled in the art that nonvolatile memory 11 can include as many configuration registers as needed to program various combinations of analog functions, digital functions, pin assignments, internal voltages, and external voltages. Moreover, one skilled in the art should recognize that a device configuration can be made dynamic such that an integrated circuit device can be re-configured during each power up or by the reception of an external control signal. Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope of the invention as set forth in the appended claims.

CLAIMS:

10. The integrated circuit of claim 9 further comprising a decoder, coupled between the one or more nonvolatile registers and a circuit configuration, for decoding the plurality of nonvolatile bits for programming analog functions.

L7: Entry 1 of 20 File: USPT Apr 6, 2004

DOCUMENT-IDENTIFIER: US 6718013 B2
TITLE: Audio recording system and method of use

Detailed Description Text (3):
The recorder-imprinter device 21 of the present invention functions to temporarily store personal audio greetings in its solid state analog memory for subsequent transfer to the permanent memory of the voice module 120, as will be discussed in detail below. The recorder-imprinter is optimally configured with a number of different input means for recording the personal audio greeting into the memory, making the device multi-functional and adaptable to the needs of all types of businesses.

L7: Entry 2 of 20 File: USPT Jun 24, 2003

DOCUMENT-IDENTIFIER: US 6581399 B2
TITLE: Apparatus and method for controlling a magnetic bearing centrifugal chiller

Detailed Description Text (7):
The chiller controller, the microprocessor computer CC 205, contains a multi-function data acquisition and control card DAQ which can accommodate both analog and digital inputs and outputs. The chiller controller also has RS-485 and RS-232 serial communications capabilities. Through the DAQ board and serial communications, the chiller controller both acquires data from the other components and sends command signals to control their operation. The DAQ board contains analog input sensor channels, analog output control signals and digital input and output ports, which are wired to external relays and configured as digital switches. The inputs acquire data from temperature sensors, pressure transducers, and/or flow rate sensors which may be located at different points throughout the chiller. From the acquired data, the CC calculates the thermodynamic conditions of the refrigerant in the evaporator and condenser. In addition, the data is used to determine if the current operating state generates an alarm or warning to alert the user of potentially unsafe conditions. FIG. 2 is a table showing the typical sensor signals connected to the analog channels for a preferred embodiment of the invention.

L7: Entry 5 of 20 File: USPT Sep 17, 2002

DOCUMENT-IDENTIFIER: US 6453175 B2
TITLE: Multi-function coding element and an associated telecommunications network

Brief Summary Text (12):
In another embodiment, the present invention is directed to a telecommunications network which includes first and second mobile terminals, each configured for transmission and receipt of digital messages in at least one of voice, facsimile and data modes, a base station controller coupled to the first and second mobile terminals by respective airlinks and an MSC configured for transmitting analog messages to, and receiving analog messages from, the base station controller in each of the voice, facsimile and data modes. The base station controller includes a multi-function coding element which converts digital voice messages into analog voice messages, analog voice messages into digital voice messages, digital facsimile messages into analog facsimile messages, analog facsimile messages into digital facsimile messages, digital data messages into analog data messages and analog data messages into digital data messages. The multi-function coding element may be comprised of plural software modules, each for performing the above-listed conversions for a particular type of message while the base station controller may include a call control resource module which controls transmissions of messages between the first mobile terminal and the MSC, transmissions of messages between the second mobile terminal and the MSC and calls to the first, second and third software modules to perform conversions on voice, facsimile and data messages, respectively.

CLAIMS:

8. A telecommunications network, comprising: a first mobile terminal; a second mobile terminal; a base station controller, said base station controller coupled to said first and second mobile terminals by respective airlinks, said first and second mobile terminals each configured for transmitting digital messages to, and receiving digital messages from, said base station controller in at least one of said voice, facsimile and data modes; and an MSC coupled to the base station controller, said MSC configured for transmitting analog messages to, and receiving analog messages from, said base station controller in each of said voice, facsimile and data modes; said base station controller including a multi-function coding element for: (a) converting digital voice messages into analog voice messages, (b) converting analog voice messages into digital voice messages; (c) converting digital facsimile messages into analog facsimile messages; (d) converting analog facsimile messages into digital facsimile messages; (e) converting digital data messages into analog data messages; and (f) converting analog data messages into digital data messages; said base station controller further including a call control resource manager for: (a) controlling exchanges of messages between said first and second mobile terminals and said MSC by receiving digital messages from said first and second mobile terminals and transferring analog conversions of said digital messages to said MSC and receiving analog messages from said MSC and transferring digital conversions of said analog messages to selected ones of said first and second mobile terminals; (b) determining whether a received message is a voice message, a facsimile message or a data message; and (c) issuing a selected call to said multi-function coding element to convert said received message based upon determining whether said received message is a voice message, a facsimile

message or a data message, wherein the messages received by the base station controller are thus processed regardless of type within the base station controller without involving an additional coding element external thereto.

L9: Entry 1 of 3 File: USPT Mar 30, 2004

DOCUMENT-IDENTIFIER: US 6714066 B2
TITLE: Integrated programmable continuous time filter with programmable capacitor arrays

Detailed Description Text (3):
Output signals from instrumentation amplifier 120 are sent to 5th order low-pass filter 130. Filter 130 is just one example of a programmable analog block that can be selectively coupled into integrated circuit 100. For example, integrated circuit 100 can include additional programmable analog blocks, for example a high-pass filter that can be programmably selected by a user and thereby coupled into a signal path. For a more general description of programmable analog integrated circuit architectures, see the aforementioned U.S. Pat. No. 5,574,678. Signals then pass from filter 130 to output amplifier 140, and to differential outputs 150.

Detailed Description Text (4):
Memory 170 and 180, which is preferably part of integrated circuit 100, store user-programmable values that specify particular filter parameters as illustrated, i.e, configuration A and configuration B. As indicated above, and further described below, the values stored typically represent settings for user selectable capacitor values, a particular combination of capacitor values yielding a corresponding set of filter parameters. Memory 170 and 180 can be implemented using static read only memory, dynamic random access memory, static random addressable memory, a serial string of shift registers, electronically erasable (E.sup.2) memory, or any other memory. Multiplexer 160 allows one of the two stored configuration to be programmed into filter 130, depending on, for example, a user command selecting one of the configurations.

Detailed Description Text (19):
Multiplexers 402, 412, and 422, along with memory 450 are used to implement the multiple filter configuration capability discussed above in conjunction with FIG. 1. Memory 450 stores pairs of configuration values A1 and B1, A2 and B2, etc., in associated memory storage elements 403 and 404, 413 and 414, etc. The configuration values represent bits used to program the various programmable capacitor arrays. The configuration of filter 130 can be quickly changed via A/B select line 440. Depending upon which configuration is selected, multiplexers 402, 412, and 422 provide values stored in memory 450 for one of the two configurations. The dual-configuration architecture need not be implemented, and thus, a single memory storage element can be associated with each user-selectable capacitor. Alternately, more than two configurations can be stored using additional memory storage elements and appropriate multiplexers. Additionally, the trim capacitors and manufacturer-controlled switches can be programmed in a manner similar to that illustrated with respect to the user-selectable capacitors. Memory 450 is preferably a static memory, such as a electronically erasable (E.sup.2) memory.

Detailed Description Text (21):
The multiple feedback paths of filter 130 and the complexity of the programmable capacitor arrays presents difficulties in testing and debugging such an integrated circuit. It is very difficult to locate a problem in the filter without breaking the feedback network. Additionally, even if the circuit performs perfectly, verifying that the programmable capacitor arrays function properly can be extremely

difficult. Consequently, it is advantageous to implement a special capacitor array test mode in the circuit for filter 130. There are two basic elements to implementing the capacitor array test mode: (1) the ability to disable one or more of the ladder filter amplifiers A1, A2, A3, A4 and A5 (i.e., to "tristate" the amplifiers) thereby deactivating certain portions of the circuit; (2) an analog interconnect array (AIC) built around the filter to reconfigure the filter into an integrator to carry-out capacitor array tests. For example, one can configure an integrator with amplifier A5 as the operational amplifier, the capacitor array under test as the feedback capacitor, and the resistors in the filter and the AIC serving as feedback and feed forward resistors. The remaining amplifiers are tristated during the test. A test signal, for example a step stimulus, is brought to the input of amplifier A5 from an input pin. By measuring the step response of the integrator (e.g., the rise time) associated with each of the capacitors in a capacitor array, one can determine if the capacitor array is behaving as designed.